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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,857	11/02/2001	David B. Fox	POU920010048US1	7451

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EXAMINER	
CHACE, CHRISTIAN	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 01/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,857	FOX ET AL.	
	Examiner	Art Unit	
	Christian P. Chace	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18* is/are allowed.

6)☒ Claim(s) *1-6 and 8-17* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet.*

Continuation of Attachment(s) 6). Other: Reasons for Allowance for claim 18.

DETAILED ACTION

Information Disclosure Statement

Information Disclosure Statement filed 2 November 2001 and entered as paper number three, has been considered by Examiner. A signed and initialed copy is attached hereto.

Drawings

Formal drawings submitted 26 February 2002 have been approved by examiner and entered as paper number two.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 11 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. While the specification technically recites the terms "broadside output" in claim 11 and "compartmentally selected output" in claim 12, neither term is described or explained in the specification in such a way as to enable one of ordinary skill in the art to make and/or use the invention. Accordingly, as examiner is currently unable to ascertain the meaning of the terms cited supra, a prior art search was not performed on claims 11 and 12 prior to issuing this Office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 8, 10, and 13-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Assouad et al (US Patent #6,119,254).

With respect to independent claim 1, a method of allocating a trace array from a cache memory is disclosed in column 2, lines 62-64. A trace array is a dedicated section [of a memory] allocated for trace data, and a data buffer is a cache.

Dividing said cache memory into a reduced-size cache memory and a trace array is disclosed in column 2, lines 62-64. If a cache is divided, one part is inherently going to be smaller than the original whole, as can be seen in figure 6, for example.

Permitting storage of trace signal data into said trace array is also disclosed in column 2, lines 62-64.

Permitting retrieval of said trace signal data from said trace array is disclosed in column 12, lines 28-30.

With respect to claim 3, said reduced-size cache memory not being equal in size to said trace array is disclose din figure 6 as well, which shows the trace array being 1/3 the size of the R/W function area of the buffer/cache.

With respect to claim 8, detecting a trace mode is disclosed in the abstract in lines 3-5, specifically.

With respect to claim 10, the combination of said reduced-size cache memory and said trace array comprising a split cache spanning the addressable space of said cache memory is, again, shown in figure 6, and further discussed in column 9, lines 15-40. Again, the cache is split into a R/W function area and a Trace Array area.

With respect to claim 13, the reduced-size cache memory and the trace array being each associated with a separate output bus is disclosed in column 2, lines 40-45, where each data port is an output bus. Also, see figure 4, where tracing data FIFO has separate bus 304 into gate 402, where microprocessor data FIFO (cache data FIFO) has bus 443 into gate 403.

With respect to claim 14, characterizing a self-timed interconnect using said trace array is disclosed in column 8, lines 27-30. (Examiner also wishes to note that a self-timed interconnect is admitted prior art in paragraph [0023] of the instant specification as well.)

Switching back to the original cache functionality once characterization is complete is disclosed in column 12, lines 53-56.

With respect to claim 15, at least one of multiplexing and time-sharing said self-timed interconnect signals with other signals to be stored in the trace array is disclosed in column 8, lines 5-6, which discloses multiplexing the signals to be stored in the trace array.

With respect to independent claim 16, a storage medium encoded with a machine-readable computer program code for allocating a trace array from an original cache memory, said storage medium including instructions for causing a computer to

implement a method [for allocating a trace array from a cache memory] is disclosed in the abstract as programmed tracing circuitry.

Dividing said cache memory into a reduced-size cache memory and a trace array is disclosed in column 2, lines 62-64. If a cache is divided, one part is inherently going to be smaller than the original whole, as can be seen in figure 6, for example.

Permitting storage of trace signal data into said trace array is also disclosed in column 2, lines 62-64.

Permitting retrieval of said trace signal data from said trace array is disclosed in column 12, lines 28-30.

With respect to independent claim 17, a computer data signal for allocating a trace array from an original cache memory, said computer signal comprising code configured to cause a computer to implement a method [for allocating a trace array from a cache memory] is disclosed in the abstract as programmed tracing circuitry.

Dividing said cache memory into a reduced-size cache memory and a trace array is disclosed in column 2, lines 62-64. If a cache is divided, one part is inherently going to be smaller than the original whole, as can be seen in figure 6, for example.

Permitting storage of trace signal data into said trace array is also disclosed in column 2, lines 62-64.

Permitting retrieval of said trace signal data from said trace array is disclosed in column 12, lines 28-30.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Assouad et al as applied to claims 1, 3, 8, 10, and 13-17 above, and further in view of Kirk (US Patent # 5,875,464).

With respect to claim 2, Assouad et al disclose the subject matter discussed supra with respect to claim 1, upon which the instant claim depends.

The difference between the instant claim and Assouad et al is the explicit recitation that the reduced-size cache is equal in size to the trace array.

However, Kirk discloses partitioning a cache in halves (where both partitions are equal) in column 15, lines 30-33.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Assouad et al and Kirk before him/her, to utilize the equal partitions of Kirk in the system of Assouad et al because this technique minimizes the required hardware, as disclosed by Kirk in column 15, line 37. In addition, Assouad et al in column 1, lines 65-67, discuss the development of single-chip technology, which requires as much reduced hardware as possible to reduce the size of the required single chip and thereby increase the speed.

With respect to claim 4, Assouad et al disclose the subject matter discussed supra with respect to claim 1, upon which the instant claim depends.

The difference between the instant claim and Assouad et al is the explicit recitation that the cache memory is 512K bytes in size. Assouad et al do disclose a memory buffer of "sufficient size" in column 3, lines 41-42.

However, Kirk discloses a 512K byte data cache, which is implicitly "sufficient," in column 9, line 67.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Assouad et al and Kirk before him/her, to utilize a 512K byte cache of Kirk in the system of Assouad et al because it is, "...of sufficient size to handle host requests," as discussed by Assouad et al in column 3, lines 40-44. Also, MPEP 2144.04 IV. A. recites:

"In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955) (Claims directed to a lumber package "of appreciable size and weight requiring handling by a lift truck" where held unpatentable over prior art lumber packages which could be lifted by hand because limitations relating to the size of the package were not sufficient to patentably distinguish over the prior art.); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976) ("mere scaling up of a prior art process capable of being scaled up, if such were the case, would not establish patentability in a claim to an old process so scaled." 531 F.2d at 1053, 189 USPQ at 148.)."

"In Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that

where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device."

With respect to claim 5, Assouad et al disclose the subject matter discussed supra with respect to claim 1, upon which the instant claim depends.

The difference between the instant claim and Assouad et al is the explicit recitation that at least one of said cache memory and said reduced-size cache memory is organized into eight-way associativities.

Kirk discloses eight-way associativity partitioning in column 12, line 46.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Assouad et al and Kirk before him/her, to utilize the eight-way associativity of Kirk in the system of Assouad et al because it can provide significantly better performance, as disclosed by Kirk in column 12, lines 50-51.

With respect to claim 6, Assouad et al disclose the subject matter discussed supra with respect to claim 1, upon which the instant claim depends.

The difference between the instant claim and Assouad et al is the explicit recitation that the cache memory comprises a directory array.

Kirk discloses a TLB, which in MIPS R3000, includes an on-chip TLB as disclosed by Kirk in column 19, line 52 and also in column 20, lines 19-24.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to utilize the TLB of Kirk in the system of Assouad et al, because

the MIPS R3000 system (which contains the TLB as discussed supra) provides support for hierarchical memory design to provide high memory bandwidth necessary to run without pipeline stalls, as discussed by Kirk in column 20, lines 41-45.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Assouad et al as applied to claims 1, 3, 8, 10, and 13-17 above, and further in view of Fischer et al (US Patent #6,376,358).

Assouad et al disclose the subject matter discussed supra with respect to claim 1, upon which the instant claim depends.

The difference between the instant claim and Assouad et al is the explicit recitation that the cache memory is comprised by a system-on-chip environment.

Fischer et al disclose a system-on-chip environment in column 1, line 18.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Assouad et al and Fischer et al before him/her, to utilize the system-on-chip environment of Fischer et al in the system of Assouad et al because the system-on-chip environment has faster speed and overcomes bandwidth and capacitance problems associated with off-chip connections, as discussed in column 1, lines 19-21 of Fischer et al.

Allowable Subject Matter

Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 18 is allowed.

The following is an examiner's statement of reasons for allowance:

With respect to allowed claim 18, the claim was drafted in a clear means-plus-function format, which invokes interpretation under 35 USC 112, sixth paragraph. This interpretation requires the details of the specification to be read into the claims. Accordingly, the cited prior art of record does not contain the exact same means for dividing and permitting, respectively, as detailed in the instant specification, and referenced by the instant claim language.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,119,254 discloses data and trace data in the same cache, used at the same time.

US 5,875,464 discloses dynamic cache partitioning for respective "tasks."

US 6,376,358 discloses a system-on-chip environment.

US 5,920,719 discloses portions of memory allocated as buffers for collecting traces.

US 2003/0126508 discloses storing debug data in dynamically allocated cache sets.

US 2002/0013877 discloses system control information dynamically allocated into cache space on-chip.

EPO 0 348 994 discloses distributed trace arrays in a hierarchical system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 703.306.5903. The examiner can normally be reached on 9-4-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on 703.308.1756. The fax phone number for the organization where this application or proceeding is assigned is 703.305.3719.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.305.3900.

Christian P. Chace